

ASX Announcement
16 June 2025**COMPANY UPDATE**

4DS Memory Limited (ASX:4DS) (4DS) (the Company) today provides an update regarding the initial internal analysis of the Sixth Platform Lot.

Highlights

- Sixth Platform Lot interim characterization testing indicates that the necessary process modifications and optimizations introduced into the Sixth Platform Lot did not yield the expected results the Company was expecting
- Electrical testing and characterization of the Sixth Platform Lot remains incomplete and will continue in the coming weeks
- Alongside finalization of Sixth Platform Lot characterization testing, the Company will perform further analysis to identify the root cause of the unexpected initial results
- If completion of testing yields no significant improvement in the function of the wafers this will likely cause a delay to the development pathway for the Company's Interface Switching ReRAM technology
- This delayed development pathway may include additional process modifications and optimisations informed by the Company's root cause analysis on the current Sixth Platform Lot

Background

On 15 January 2025, the Company announced the completion of the testing and characterization of the Fifth Platform Lot. The purpose of the Fifth Platform Lot was to optimize the construction process of memory cell arrays to de-risk the manufacturing of the first 4DS 20nm memory cell arrays incorporated in the Sixth Platform lot.

Using the proven cell size of 60nm array (demonstrated in the Fourth Platform Lot), the Fifth Platform Lot sought to uncover any processing issues that could arise when adjusting the memory cell stack necessary for successful construction of the 20nm memory cell array in the Sixth Platform Lot.

After extensive electrical testing including chemical and physical cross-sectional analysis, key areas of optimization were identified and shared with the imec engineering team working on the Sixth Platform Lot.

The key process learnings from the Fifth Platform Lot that were necessary for scaling of the memory cell array from 60nm cells to 20nm cells (9 times smaller in area) and the focus of the Sixth Platform Lot was:

- Memory cell array patterning and etching: new process tuning modifications for the construction of 20nm cells.

- Memory stack adjustment: the advanced memory stacks which are necessary for the construction of 20nm cells have shown functionality and which de-risks the Sixth Platform Lot with similar memory cell stack constructions.
- Memory array process integration: the best options of the post-patterning backend processes of the advanced memory cells were selected and implemented to the Sixth Platform Lot.

These new learnings and optimizations from the Fifth Platform Lot were important for the successful manufacturing and processing of 4DS's first 20nm memory cell array in the Sixth Platform Lot, which has now been manufactured and analyzed in 1H 2025 as previously guided.

Sixth Platform Lot Initial Analysis

On 28 April 2025, the Company announced that imec had successfully completed the manufacturing and processing of the Sixth Platform Lot. This Lot was received at the 4DS facilities in Fremont on 6 May 2025 and electrical testing started the next day.

While electrical testing and characterization of the Sixth Platform Lot is still incomplete and will continue for a few more weeks, the initial analysis of the wafers within the entire Lot indicates that the necessary process modifications and optimizations introduced into the Sixth Platform Lot have not yielded the expected electrical testing and characterization results the Company was expecting.

The Company will now perform a root cause analysis which includes further electrical testing, physical analytics and chemical analysis to identify the reasons for the unexpected initial analysis in the 20nm Sixth Platform Lot to date.

If over the coming few weeks, the initial analysis seen to date remains similar or 4DS evidences no significant improvement in the function of the wafers this will likely cause a delay to the development pathway for the Company's Interface Switching ReRAM technology.

This delayed development pathway may include additional process modifications and optimisations informed by the Company's root cause analysis on the current Sixth Platform Lot.

Executive Chairman Mr. David McAuliffe commented "The initial analysis of the Sixth Platform Lot will now be shared and discussed with imec and Infineon Technologies Inc. The Company intends to create updated development plans and timelines following these discussions and the completion of the extensive electrical testing and characterization of the Sixth Platform Lot."

Company Update

The Company currently has approximately \$10 million in available funds so is well funded. The Company will be hosting an investor webinar in the coming weeks to provide further updates on the outcome of the Sixth Platform Lot analysis. Details of the webinar will be announced soon.

Authorised for release by the Board.

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About 4DS

4DS Memory Limited (ASX: 4DS), with facilities located in Silicon Valley, is a semiconductor technology company bringing high bandwidth, high endurance, persistent non-volatile memory to advanced CMOS process nodes. Its technology, known as Interface Switching ReRAM, features tuneable persistence and low energy per bit for today's most challenging compute intensive and AI processor applications.

Established in 2007, 4DS owns a patented IP portfolio, comprising 34 USA patents, and is the first company to develop PCMO ReRAM, on an advanced CMOS processing node. 4DS has three important industry relationships: a development agreement with Belgium based imec, a world leading research and innovation hub in nano electronics and digital technologies; a design agreement with Infineon Technologies AG, Germany's largest semiconductor manufacturer and one of the ten largest semiconductor manufacturers worldwide; and a joint development agreement with Western Digital subsidiary HGST, a global leader in storage solutions.

For more information, please visit www.4dsmemory.com.